

**Chapter 1 : Introduction to Advanced Digital Design****1-1 to 1-33****Syllabus**

- Comparison of BJT and CMOS parameters
- Design of Basic gates using CMOS : Inverter, NOR, NAND, MOS transistor switches, transmission gates.
- Drawing of complex logic using CMOS (building of logic gate as per the Boolean equation of three variable).
- Estimation of layout resistance and capacitance, switching characteristics.
- Fabrication process : Overview of wafer processing, Oxidation, epitaxy, deposition, Ion-Implementation and diffusion, silicon gate process.
- Basics of NMOS, PMOS and CMOS: nwell, pwell, twin tub process.

| | | |
|-------|---|-----|
| 1.1 | Introduction..... | 1-1 |
| 1.2 | Terminologies used in Sequential Logic..... | 1-1 |
| 1.2.1 | Metastability..... | 1-1 |
| 1.2.2 | Noise Margins..... | 1-2 |
| 1.2.3 | Fan-out..... | 1-2 |
| 1.2.4 | Clock..... | 1-2 |
| 1.2.5 | Clock Skew..... | 1-2 |
| 1.2.6 | State..... | 1-2 |
| 1.2.7 | State Table..... | 1-3 |
| 1.2.8 | State Diagram..... | 1-3 |
| 1.3 | Flip-Flops..... | 1-3 |
| 1.3.1 | S-R Latch..... | 1-3 |
| 1.3.2 | D-Flip Flop..... | 1-4 |
| 1.3.3 | J-K Flip-Flop..... | 1-4 |
| 1.3.4 | T Flip-Flop..... | 1-5 |
| 1.4 | What is State Machine ?..... | 1-6 |

| | | |
|--------|---|------|
| 1.4.1 | State Machine Structure..... | 1-7 |
| 1.4.2 | Comparison of Moore and Mealy FSM..... | 1-7 |
| 1.5 | Analysis of the State Machine..... | 1-8 |
| 1.5.1 | Analysis of the State Machines with D-Flip-Flop..... | 1-8 |
| 1.5.2 | Analysis of the State Machines with JK Flip-flop..... | 1-10 |
| 1.5.3 | Analysis of the State Machines with T-Flip-Flop..... | 1-11 |
| 1.6 | Clock Synchronous State Machine Design..... | 1-15 |
| 1.6.1 | Comparison between Synchronous and Asynchronous Sequential Circuit..... | 1-22 |
| 1.7 | Introduction to ASIC..... | 1-23 |
| 1.8 | ASIC Design Flow..... | 1-23 |
| 1.9 | EDA Tools..... | 1-24 |
| 1.9.1 | Front End Design Tools for FPGA and ASIC Flow..... | 1-24 |
| 1.9.2 | Back End Design Tools for FPGA..... | 1-24 |
| 1.9.3 | Back End Design Tools for ASIC..... | 1-25 |
| 1.10 | Programmable Logic Devices (PLDs)..... | 1-25 |
| 1.11 | Complex Programmable Logic Devices (CPLD)..... | 1-25 |
| 1.12 | Xilinx XC 9500 CPLD Family..... | 1-26 |
| 1.12.1 | Xilinx XC9500 CPLD Family Architecture..... | 1-26 |
| 1.12.2 | Function Block Architecture..... | 1-27 |
| 1.12.3 | XC 9500 Product Term Allocator and Macrocell..... | 1-27 |
| 1.12.4 | Input / Output- Block Architecture..... | 1-28 |
| 1.12.5 | Switch Matrix..... | 1-29 |
| 1.13 | ATMEL CPLD Family..... | 1-29 |
| 1.14 | Field Programmable Gate Arrays (FPGA)..... | 1-29 |
| 1.15 | Features of FPGA..... | 1-29 |
| 1.16 | Xilinx XC 4000 FPGA Family..... | 1-29 |
| 1.16.1 | Configurable Logic Block..... | 1-30 |



| | | | | | |
|---|--|------|--------|---|------|
| 1.16.2 | Input/Output Block..... | 1-30 | 2.3.2 | MOSFET Inverter with E-nMOS as Pull Up..... | 2-3 |
| 1.16.3 | Programmable Interconnect..... | 1-31 | 2.3.3 | MOSFET Inverter with D-nMOS as Pull Up..... | 2-4 |
| 1.17 | FPGA-SPARTAN-3 Series..... | 1-31 | 2.3.4 | MOSFET Inverter with pMOS in Pull Up i.e. CMOS Inverter..... | 2-4 |
| 1.17.1 | Introduction to FPGA-SPARTAN-3 Series..... | 1-31 | 2.4 | Active Load NAND and NOR Gates..... | 2-5 |
| 1.17.2 | Features of SPARTAN-3 Series..... | 1-31 | 2.4.1 | CMOS NAND Gate..... | 2-6 |
| 1.17.3 | Spartan 3 Family Architecture..... | 1-32 | 2.4.2 | CMOS NOR Gate..... | 2-8 |
| 1.17.4 | Architectural Overview..... | 1-32 | 2.5 | Transmission Gate..... | 2-9 |
| 1.18 | ATMEL Series FPGAs..... | 1-32 | 2.6 | Realization of any Boolean Equation using N-MOS and C-MOS..... | 2-9 |
| 1.19 | Comparison between FPGA and CPLD..... | 1-33 | 2.7 | Circuit Elements..... | 2-13 |
| 1.20 | Xilinx and ATMEL Series Architecture for CPLD..... | 1-33 | 2.7.1 | Resistors..... | 2-13 |
| Chapter 2 : Introduction to CMOS Technology | | | 2.7.2 | Capacitors..... | 2-13 |
| 2-1 to 2-27 | | | 2.8 | MOS Circuit Characterization and Performance Estimation..... | 2-13 |
| Syllabus | | | 2.9 | Resistance Estimation..... | 2-13 |
| – Comparison of BJT and CMOS parameters | | | 2.10 | Capacitance Estimation..... | 2-15 |
| – Design of Basic gates using CMOS : Inverter, NOR, NAND, MOS transistor switches, transmission gates. | | | 2.10.1 | MOS- Capacitor Characteristics (C-V Characteristics)..... | 2-15 |
| – Drawing of complex logic using CMOS (building of logic gate as per the Boolean equation of three variable). | | | 2.10.2 | MOS Device Capacitance..... | 2-16 |
| – Estimation of layout resistance and capacitance, switching characteristics. | | | 2.10.3 | Oxide Related Capacitances..... | 2-16 |
| – Fabrication process : Overview of wafer processing, Oxidation, epitaxy, deposition, Ion-Implementation and diffusion, silicon gate process. | | | 2.10.4 | Junction Capacitance..... | 2-17 |
| – Basics of NMOS, PMOS and CMOS: nwell, pwell, twin tub process. | | | 2.10.5 | Routing Capacitance..... | 2-18 |
| 2.1 | Comparison Between BJT and CMOS..... | 2-1 | 2.11 | Switch Characteristics..... | 2-18 |
| 2.2 | Design of Basic Gates Using CMOS..... | 2-1 | 2.11.1 | Rise Time Estimation..... | 2-19 |
| 2.2.1 | MOS Transistor Switches..... | 2-1 | 2.11.2 | Fall Time Estimation..... | 2-19 |
| 2.2.2 | Basic MOS Inverter..... | 2-2 | 2.11.3 | Delay Time (t_d)..... | 2-20 |
| 2.3 | Types of MOS Inverters..... | 2-2 | 2.12 | Fabrication Process..... | 2-20 |
| 2.3.1 | D-nMOS Inverter with Resistive Load..... | 2-3 | 2.12.1 | Wafer Processing..... | 2-20 |
| | | | 2.12.2 | Oxidation..... | 2-21 |
| | | | 2.12.3 | Epitaxial Growth..... | 2-21 |
| | | | 2.12.4 | Deposition..... | 2-21 |
| | | | 2.12.5 | Diffusion..... | 2-21 |



| | | | | | |
|--------|---|------|-------|-------------------------------|-----|
| 2.12.6 | Ion Implantation | 2-21 | 3.7 | Operators | 3-6 |
| 2.12.7 | Lithography | 2-22 | 3.7.1 | Logical Operators | 3-6 |
| 2.12.8 | Etching | 2-22 | 3.7.2 | Relational Operators | 3-6 |
| 2.12.9 | Metallization | 2-22 | 3.7.3 | Shift Operators | 3-6 |
| 2.13 | nMOS Fabrication | 2-22 | 3.7.4 | Adding Operators | 3-6 |
| 2.14 | pMOS Transistor Fabrication Process | 2-23 | 3.7.5 | Multiplying Operators | 3-7 |
| 2.15 | Basic CMOS Technology | 2-24 | 3.7.6 | Miscellaneous Operators | 3-7 |
| 2.15.1 | The P Well Process | 2-24 | 3.8 | Configurations | 3-7 |
| 2.15.2 | The N- Well Process | 2-25 | 3.8.1 | Default Configuration | 3-7 |
| 2.15.3 | Latch up in CMOS | 2-26 | | | |
| 2.15.4 | CMOS using Twin Tub Process | 2-26 | | | |

Chapter 3 : Introduction to VHDL 3-1 to 3-8

Syllabus

- Introduction to HDL: History of VHDL, Pro's and Con's of VHDL.
- VHDL Flow elements of VHDL(Entity, Architecture, configuration, package, library only definitions)
- Data Types, operators, operations
- Signal, constant and variables (syntax and use).

| | | |
|-------|-------------------------------|-----|
| 3.1 | Introduction | 3-1 |
| 3.2 | What is VHDL ? | 3-1 |
| 3.2.1 | Pro's of VHDL Languages | 3-1 |
| 3.2.2 | Con's of VHDL | 3-1 |
| 3.2.3 | VHDL Terms | 3-2 |
| 3.2.4 | Features of VHDL | 3-3 |
| 3.3 | VHDL Representation | 3-3 |
| 3.4 | Sequential Processing | 3-3 |
| 3.5 | Data Objects | 3-4 |
| 3.6 | Data Types | 3-4 |
| 3.6.1 | Scalar Data Types | 3-4 |
| 3.6.2 | Composite Types | 3-5 |

Chapter 4 : VHDL Programming 4-1 to 4-24

Syllabus

- Concurrent constructs (when, with, process).
- Sequential Constructs (process, if, case, loop, assert, wait).
- Simple VHDL program to implement Flip Flop, Counter, shift register, MUX, DEMUX, ENCODER, DECODER, MOORE, MEALY machines.
- Test bench and its applications.

| | | |
|-------|--|-----|
| 4.1 | Introduction | 4-1 |
| 4.2 | Different Styles of Modeling | 4-1 |
| 4.2.1 | Data Flow Modeling | 4-1 |
| 4.2.2 | Behavioural Modeling | 4-2 |
| 4.2.3 | Structural Modeling | 4-2 |
| 4.3 | Modeling Simple Elements | 4-3 |
| 4.4 | Modeling Conditional Operators | 4-4 |
| 4.5 | Modeling Combinational Logic | 4-5 |
| 4.6 | Modeling Regular Structure | 4-5 |
| 4.7 | Modeling Synchronous Logic | 4-6 |
| 4.8 | Comparison of Different Modelling Styles | 4-7 |
| 4.9 | Concurrent Constructs (Statements) | 4-7 |
| 4.9.1 | With Select Statement | 4-7 |
| 4.9.2 | When_Else Statement | 4-8 |



| | | | | | |
|--|--|------|-------|--|------|
| 4.9.3 | Generate Statements..... | 4-9 | 5.4 | Zero Modeling..... | 5-2 |
| 4.10 | Sequential Processing..... | 4-9 | 5.5 | Simulation Cycle..... | 5-2 |
| 4.10.1 | Process Statement..... | 4-9 | 5.5.1 | Simulation..... | 5-2 |
| 4.10.2 | Sequential Statements..... | 4-10 | 5.5.2 | Steps in Simulation..... | 5-3 |
| 4.10.3 | If Statement..... | 4-10 | 5.5.3 | Simulation Process..... | 5-3 |
| 4.10.4 | Case Statement..... | 4-11 | 5.5.4 | Simulation Deltas..... | 5-3 |
| 4.10.5 | Loop Statement..... | 4-12 | 5.6 | Comparison of Software and Hardware Description Language..... | 5-5 |
| 4.10.6 | Null Statement..... | 4-12 | 5.7 | Delta Delay in Simulation..... | 5-5 |
| 4.10.7 | Exit Statement..... | 4-12 | 5.7.1 | Inertial and Transport Delay..... | 5-5 |
| 4.10.8 | Next Statement..... | 4-13 | 5.8 | Simulation and Types of Simulator..... | 5-6 |
| 4.10.9 | Wait Statement..... | 4-13 | 5.8.1 | Simulation..... | 5-6 |
| 4.10.10 | Comparison between Concurrent and Sequential Statement..... | 4-14 | 5.8.2 | Types of Simulator..... | 5-6 |
| 4.11 | Examples Using VHDL..... | 4-14 | 5.9 | HDL Design Flow for Synthesis..... | 5-6 |
| 4.12 | Test Bench..... | 4-22 | 5.9.1 | Synthesis Issues..... | 5-6 |
| 4.12.1 | Test Bench for Testing D-flip flop..... | 4-22 | 5.9.2 | Design Synthesis..... | 5-7 |
| 4.12.2 | Verification using Test Benches..... | 4-23 | 5.9.3 | Flattening..... | 5-8 |
| 4.12.3 | Waveform Generation..... | 4-23 | 5.9.4 | Structuring..... | 5-8 |
| 4.12.4 | Assertion Statements..... | 4-23 | 5.9.5 | Synthesis Process - Review..... | 5-8 |
| Chapter 5 : HDL Simulation and Synthesis 5-1 to 5-10 | | | 5.9.6 | Synthesis Tools Expectation..... | 5-9 |
| Syllabus | | | 5.9.7 | Synthesis Tools Features..... | 5-9 |
| <ul style="list-style-type: none"> – Event scheduling, sensitivity list, zero modeling, simulation cycle, comparison of software and hardware description language, delta delay, Types of simulator event based and cycle based. – HDL Design flow for synthesis. – Efficient Coding Styles, Optimizing arithmetic expression, sharing of complex operator. | | | 5.9.8 | Use of Synthesis and Simulation in VHDL..... | 5-9 |
| 5.1 | VLSI Design Flow..... | 5-1 | 5.9.9 | Good Coding Practices..... | 5-9 |
| 5.2 | Event Scheduling..... | 5-1 | 5.10 | Efficient Coding Styles..... | 5-9 |
| 5.3 | Sensitivity List..... | 5-2 | 5.11 | Optimizing Arithmetic Expressions in VHDL..... | 5-10 |
| | | | 5.12 | Sharing of Complex Operators..... | 5-10 |